Electrically Tunable Silicon 2-D Photonic Bandgap Structures

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Abstract—Electrical tuning of high refractive index-contrast photonic bandgap (PBG) structures is required for a majority of PBG applications, particularly for integrated optics. When the host material is a semiconductor with poor electro-optical properties, tuning can be achieved by infiltrating the structure with an active optical material. In this paper we analyze the switching of electro-optic material in such structures, and suggest design rules to help achieve electrical tuning. In particular, a design concept that eliminates the electric field screening effects is proposed. The developed rules and concepts are demonstrated by the electrical tuning of liquid crystals inside two-dimensional porous silicon PBG structures. This approach can be generalized to different combinations of semiconductor PBG structures and active optical materials.

Index Terms—Electro-optic material, field screening, liquid crystals, photonic bandgap (PBG), silicon.

I. INTRODUCTION

High refractive index-contrast photonic crystals, often realized in semiconductor materials, possess strong light confinement capabilities and large bandgaps. They have great potential in applications ranging from biosensors [1] to on-chip optical interconnects [2], where the ability to control the properties of light is critical.

Photonic crystals are periodic dielectric structures. As a result of this periodicity, photonic crystals can be designed to exhibit photonic bandgap (PBG) structures, in much the same way as solid-state crystalline materials exhibit electronic bandgaps [3]. The corresponding reflectance spectra of such PBG structures, can be exploited to manipulate the propagation of light. Many novel photonic devices have already been built or proposed, including planar superprisms [4], ultracompact add-drop filters [5], and slow group velocity microcavity arrays [6]. However, the full potential of these structures can only be realized if their photonic properties can be tuned.

Because the two-dimensional (2-D) PBG structures are most often fabricated by etching pores into a dielectric host material, perhaps the most straightforward way to enable tunability is to fill the pores with an active electro-optic material. Thus, by changing the refractive index of the active material, the reflectance spectrum of the PBG structure can be changed. This approach is especially attractive because it decouples the physical limitations of the host and active materials. Thus, we are free to fabricate the host structure using one material, for example silicon, in order to maintain compatibility with the existing semiconductor manufacturing infrastructure, and to infiltrate the device with an electro-optic material at the last stage of fabrication to enable tunability. In this way, tuning the PBG structure simply requires the application of an electrical signal to the active material. However, despite numerous attempts at electrical switching in such high index-contrast 2-D PBG structures, there are still no successful reports of it in the literature. The main obstacle common to all the semiconductor materials is the electric field screening inside the pores due to the conductive host walls. The experimental consequences of this screening were most recently observed in liquid-crystal (LC)-filled PBG lasers [7], where only the surface layer of LCs could be switched, thus greatly reducing the tuning efficiency.

In this paper, we propose and demonstrate a design methodology to essentially eliminate field screening effects, thus enabling efficient tuning. This methodology can be applied across various combinations of semiconductor PBG structures and active optical materials.

II. ELECTRIC FIELD PBG SWITCHING: ANALYSIS AND DESIGN CONSIDERATIONS

A. Device Geometry: Equivalent Circuit Analysis

The 2-D PBG structures referred to in this analysis are regular arrangements of cylindrical holes, or pores that have been etched into a semiconductor host. The particular structure to be analyzed consists of a silicon host and LC-filled pores that are arranged in a hexagonal (also called triangular) lattice. In this study, silicon was chosen as the host material for two reasons: first, to take advantage of the existing semiconductor manufacturing infrastructure and ensure compatibility with standard electronic devices; and second, because silicon allows for a very high resolution in the fabricated structure. The active material chosen was E7 nematic LC because of its high birefringence. Nevertheless, the analysis can be generalized to other geometries and material systems.

A voltage applied across the length of the pores, i.e., between the top aluminum contact and the back of the silicon wafer, would ideally cause the LCs to reorient, thus causing a change in their refractive index that, in turn, would change the reflectance spectrum of the PBG device. In practice, however, the applied electric field can be screened out of the LC by the silicon host, because the conductivity of silicon is several orders of magnitude higher than that of the LC.
magnitude higher than that of the LC. The result is that the field distribution within the pores is nonuniform, and only a small fraction of the LC molecules experience a field large enough to reorient. This effect is referred to as electric field screening, and is a well-known phenomenon \[9\].

While the problem of pore-wall conductivity is often mentioned \[7\], another important issue is often overlooked—the placement and geometry of the electrical contacts. Analysis of the field distribution inside composite structures such as PBG devices is complex and often not intuitive. To understand the physics behind such a structure, it is helpful to build a model of its operation. Simple electrical engineering methods, such as equivalent circuit analysis, perform surprisingly well in this case.

For example, Fig. 1(a) shows a typical device configuration used for LC tuning. Here, the external electric field is applied between the silicon substrate and an external electrode, typically an ITO-coated glass, with an LC-filled 2-D PBG structure sandwiched in between. Because of the nonplanarity of the substrate and the ITO glass, there is a thin layer of LC material sandwiched in between. Because of the nonplanarity of the substrate and the ITO glass, there is a thin layer of LC material sandwiched between the PBG structure and the top contact. The simulated field profile reveals that the electric field amplitude inside the pores is significantly reduced as compared to the bulk LC layer even in the case of complete silicon depletions.

The electrical characteristics of the device can be expressed in the form of the equivalent circuit shown just to the right of the cross-sectional view in Fig. 1(b). This circuit helps to illustrate the two problems that cause electric field screening in this configuration: the impedance \(Z_T\) of the LC layer on top of the PBG, and the field leakage into the conductive pore walls \(I_X\). By a simple circuit analysis, the voltage drop on the surface LC layer \(V_T\) can be expressed as

\[
V_T = \frac{1}{K} \left( V_{\text{ext}} Z_T (Z_{\text{LC}} + Z_{\text{Si}})^2 Z_T + (Z_{\text{LC}} + Z_{\text{Si}})(Z_{\text{Si}} + 3Z_T)Z_X + (2Z_{\text{Si}} + Z_T)Z_X^2 \right) \tag{1}
\]

where \(V_{\text{ext}}\) is the voltage applied between the electrical contacts, \(Z_{\text{LC}}\) is the impedance of LCs inside the pore, \(Z_{\text{Si}}\) is impedance of silicon, and \(Z_X\) is the lateral impedance between the LCs and silicon host. The leakage current can be expressed as

\[
I_X = \frac{(Z_{\text{LC}} - Z_{\text{Si}})Z_T Z_X V_{\text{ext}}}{K} \tag{2}
\]

where \(K\) is given by

\[
K = (2Z_{\text{LC}} + Z_T)(2Z_{\text{Si}} + Z_T)Z_X^2 + (Z_{\text{LC}} + Z_{\text{Si}})Z_T(4Z_{\text{LC}}Z_{\text{Si}} + (Z_{\text{LC}} + Z_{\text{Si}})Z_T) + \{(2Z_{\text{LC}}Z_{\text{Si}} + 3Z_T^2)(Z_{\text{LC}} + Z_{\text{Si}}) + (Z_{\text{LC}}^2 + 12Z_{\text{LC}}Z_{\text{Si}} + Z_{\text{Si}}^2)Z_X^2\} \tag{3}
\]

To eliminate the electric field screening, the current leakage from LCs to silicon should be equal to or less than zero. Setting \(I_X\) less than or equal to zero and solving (1) and (2) for \(Z_T\) if \(Z_{\text{LC}} > Z_{\text{Si}}\) results in the unique solution \(Z_T = 0\). Therefore, the only way to avoid the electric field screening is to eliminate the impedance of the surface layer of the LCs. Experimentally, this can be realized by placing a continuous electrode on top of the PBG structure, in direct contact with both the top of the pore walls and LCs.

Physical deposition (evaporation or sputtering) of electrodes is preferred as it ensures direct contact with the silicon. Because of the high temperatures involved in physical deposition, it is not possible to deposit a contact onto the infiltrated PBG structure without destroying the LC. Therefore, the electrodes must be placed only on top of the silicon, to allow LC infiltration into the pores after contact evaporation. Simulations of the electric field in such a geometry reveal a uniform field distribution, as shown in Fig. 1(c). From the equivalent circuit analysis, the field inside the active region of such a device comes from the current flow through the lateral impedance \(Z_X\)

\[
I_X = \frac{Z_T V_{\text{ext}}}{2Z_{\text{LC}}^2 + 2Z_{\text{Si}}^2 + 2Z_{\text{Si}}Z_T + 2Z_X^2}. \tag{4}
\]

Note that \(I_X\) is negative for this geometry. This indicates an “inverse” electric field screening effect, where the electric field direction is opposite to the applied voltage.
field leaks into the active region from the conductive silicon host. The field simulation in Fig. 1(c) illustrates that there is indeed no electric field attenuation in the active region for this configuration. Despite the fact that the contact is only deposited on the silicon host, the result is a uniform field distribution throughout the entire active region.

Intuitively, an even better solution to the electric field screening problem would be to fabricate an insulated PBG membrane by coating it with a layer of dielectric (for example, silicon dioxide), and to then form electrical contacts on both sides of the structure. However, Fig. 1(d) shows that such a geometry does not result in a uniform field distribution. The silicon dioxide coating acts as a capacitor, providing a current path into the conductive host walls and around the high-impedance LCs, as shown in the equivalent circuit. The result is an attenuation of the electric field toward the center of the active region, which is most often the location of the center of the optical mode.

It can be seen from the analysis above that in order to achieve a uniform electric field distribution inside the high-resistivity active region, it is necessary to provide a direct contact to the low-resistivity semiconductor host.

Another interesting and practical example of the proposed concept is the lateral electrode configuration shown in Fig. 2. In this configuration, the voltage is applied laterally between the two contacts that are in direct contact with the silicon host according to the rule derived earlier. The equivalent circuit in this figure identifies two major current paths through the structure. In the first case, the current passes directly through the silicon walls (right arm). The second current path, which intersects the pores, consists of the alternating areas of LCs and silicon. Because of the complex geometry, the cross-talk impedance $Z_X$ between those two paths can change anywhere between $Z_X = Z_{LC}$ to $Z_X = Z_{Si}$. To estimate the electric field distribution, we can analyze the circuit at both extremes. From the equivalent circuit, the ratio of the voltage drops across $Z_{LC}$ and $Z_{Si}$ can be written as

$$V_{LC}/V_{Si} = \frac{Z_{LC}^2(Z_{LC} + 4Z_{Si})}{Z_{Si}(Z_{LC}^2 + 3Z_{LC}Z_{Si} + Z_{Si}^2)}, \quad Z_X = Z_{LC}$$

(5)

$$V_{LC}/V_{Si} = \frac{Z_{LC}(3Z_{LC} + 2Z_{Si})}{Z_{Si}(2Z_{LC} + 3Z_{Si})}, \quad Z_X = Z_{Si}.$$  

(6)

If $Z_{LC} > Z_{Si}$, the voltage across the LC-filled pore is actually higher than the voltage across the adjacent silicon wall for both extremes, which indicates the field concentration inside the LC material. Such a configuration allows for the creation of a lateral electric field. The simulated field distribution confirms the field enhancement inside the LC, as derived in the equivalent circuit analysis.

### B. Reducing the Conductivity of the PBG Host

While the concept proposed in Section II-A results in a uniform field distribution throughout the structure, it may also lead to an increased current through the device. To avoid excessive power consumption, it is necessary to utilize the properties of the semiconductor host to lower the pore-wall conductivity. The conductivity of a semiconductor material can be expressed as

$$\sigma = qn\mu_n + qp\mu_p$$  

(7)

where $n$ and $p$ are the concentrations, and $\mu_n$ and $\mu_p$ are the mobilities of free electrons and holes, respectively. There are two main phenomena that influence the conductivity of the pore walls.

1) The minority carrier concentration can be significantly reduced by the lateral space-charge region surrounding each pore. The width of the space charge region depends on the surface states, electrochemical potential (or Fermi level) of the material inside the pore, silicon doping, etc. In case of complete overlap of lateral space charge regions of adjacent pores, the pore wall is completely depleted of majority carriers, and has a resistivity close to that of the intrinsic silicon. The width of the space-charge region can be maximized by an appropriate surface treatment, by applying an external bias, or by manipulating the electrochemical potential of the active material.

2) The free-carrier mobility can be lowered by the carrier scattering events. This phenomenon is well known in complementary metal–oxide–semiconductor (CMOS) transistors, where carrier mobility in the channel can be five to ten times lower than the bulk value. Artificial surface and bulk traps can help in minimizing the carrier mobility.

The width of the space charge region in the PBG structure may be difficult to calculate precisely owing to the unknown electronic properties of the active material on the other side of the interface. In this paper, a thin layer of silicon dioxide is assumed to coat the pore-wall surface, which is typical of silicon surfaces. One way to estimate the width of the space charge region in this case is to strike a balance between the space charge in the semiconductor, and the fixed surface charge density in the oxide, which for CMOS-quality oxide is to the order of $10^{-12}$ cm$^{-3}$ [10]

$$\int n_{surf} dS = \int V_{SCR} dV$$  

(8)

which under normal conditions can be approximated as

$$n_{surf} S_{ox} = N_d V_{SCR}$$  

(9)
where \( n_{\text{surf}} \) is the surface density of charges on the oxide, \( n_{\text{SCR}} \) the volume charge density inside the space-charge region, \( S_{\text{ox}} \) the surface area, \( N_d \) the level of the semiconductor doping, and \( V_{\text{SCR}} \) the volume of the space-charge region.

When (8) requires the space-charge region to extend throughout the whole pore-wall thickness, the host has a resistivity close to that of intrinsic silicon, \( 4 \times 10^{-5} \) (\( \Omega \cdot \text{cm} \))\(^{-1} \). To minimize current through the structure, it is necessary to choose the surface area to volume ratio that results in a complete overlap between the space-charge regions of the adjacent pores. The ratio between the pore radius \( r \) and lattice constant \( a \) is often used in the design of PBG structures. As an example, Fig. 3 shows the minimum \( r/a \) ratio required for complete depletion as a function of lattice constant for the triangular pore lattice, used in this paper.

Mobility modification due to scattering events is more difficult to estimate, as it depends on both the pore-wall dimensions and the built-in local fields. For example, highly doped semiconductors have a higher concentration of scattering centers and thus a lower mobility. However, a more highly doped semiconductor may have a lower conductivity in the depleted state than a lower doped semiconductor.

Both structure geometry and material properties need to be optimized to allow for efficient tunable PBG structures. The geometry must ensure a direct current path through the low-resistivity semiconductor host. To minimize the power consumption, the resistivity of the semiconductor needs to be maximized by lowering the free-carrier concentration and mobility.

III. EXPERIMENT

PBG structures were fabricated using the macroporous etching of interferometrically prestructured silicon substrates [11]. Following the etching, the necessary \( r/a \) ratio was achieved by sample oxidation and subsequent hydrofluoric (HF) etching cycles. In accordance with the calculations in Section II-B, the \( r/a \) ratio was set to 0.42. To facilitate the application of an electric field, aluminum contacts were formed on both sides of the sample by thermal evaporation. The aluminum contacts were subsequently annealed to provide a direct ohmic contact to the silicon host, as discussed in Section II-A. To ensure a homeotropic alignment of the LCs (i.e., perpendicular to the pore walls), the PBG structures were treated with an n-methylphenylsiloxane solution [12]. Finally, the LCs were introduced into the pores in the isotropic state through the use of capillary forces. Experimental details can be found in [13].

The pore diameter of the fabricated PBG structures is 1 \( \mu \text{m} \), and the thickness of the porous layer was set to either 15 or 60 \( \mu \text{m} \). For samples with such high aspect ratios, even a weak free-carrier electric field screening can significantly attenuate the electric field strength inside the pores. To experimentally demonstrate the concepts outlined in Section II, two different techniques were used to monitor the optical response to tuning by the electric field.

1) A polarized light microscope was used to analyze the birefringence of the samples in the direction perpendicular to the 2-D PBG plane. With this technique, the actual switching of LC molecules inside the PBG structure can be observed. In order to accommodate for the transmission measurement using visible light, the opaque silicon substrate was removed by anisotropic chemical etching. The resulting silicon PBG membrane suspended in a silicon wafer frame is shown in Fig. 4(a).
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2) A Fourier transform infrared (FTIR) microscope was used to measure the reflection in the plane of the PBG structure. This technique demonstrates the actual electrical tuning of photonic bands, which can be directly used for light modulation in integrated devices. To allow for reflectance measurements, the sample was cleaved along one of the photonic crystal planes to expose the PBG face. Because of the signal to noise ratio requirements, the PBG structure must be at least 50–60 µm thick to allow for a sufficiently large measurement spot area.

IV. RESULTS AND ANALYSIS

For the polarized light microscopy investigation the PBG sample was placed between two crossed polarizers, with the pores parallel to the direction of light propagation. In the case where the LC material is oriented so that its optical axis is coincident with the light propagation direction, no birefringence is produced, the polarization state of the transmitted light remains unchanged, and thus no light is transmitted. Optical birefringence produced by the reorientation of the LC optical axis changes the polarization state of the light passing through the sample, and thus some portion of it is transmitted through the second polarizer. By measuring the intensity of the transmitted light, it is possible to estimate the value of the optical birefringence.

A charge-coupled device (CCD) camera was used to monitor the intensity of the polarized light component that passed through the porous silicon membrane as a function of applied electrical voltage. The applied voltage was a sinusoidal signal with a frequency of 1 kHz. The resulting dependence of the transmitted light intensity versus the applied voltage is shown in Fig. 5 (solid line). At \( V_{rms} = 11.5 \text{ V} \), a significant decrease in light intensity is clearly observed as the LC molecules align themselves to be parallel to the electric field lines. The birefringence of the LC is at or near its minimum value in this state, which decreases the light transmission through the microscope.

Fig. 5 also shows the transmission of unpolarized light as a function of external voltage (dotted line). The intensity of the transmitted light increases with the voltage due to the lower scattering losses produced by the long-range orientational ordering effect of the applied electric field. This measurement suggests that the curve obtained with the crossed polarizers (solid line) is a superposition of two effects: initially, the reduced scattering increases the transmission at moderate voltages, but near the phase transition, the polarization effect takes over to abruptly reduce the transmitted light intensity.

To study the photonic properties of tunable PBG structures, an FTIR spectrometer was used to measure the reflection in the plane of the PBG layer. A wire-grid polarizer was used to control the polarization of the probe light to be parallel to the pore axes (transverse magnetic (TM) polarization). For this polarization of light, the LC molecules oriented perpendicular to the pore axes appear as a low refractive index material, while the LCs oriented parallel to the pore axes appear as a high refractive index material. Fig. 6 shows the shift of the higher energy TM band edge as a function of applied voltage. This band edge is defined by the second photonic band, with its energy concentrated inside the LC columns. The observed shift is due to the LC reorientation along the electric field lines, which increases the average LC refractive index for the TM polarized light. The bandgap edge shift exceeds the theoretically predicted value owing to the experimental error. In contrast, the lower energy edge of the first-order bandgap, where the electromagnetic field is concentrated inside the silicon host, does not change with the applied voltage within the experimental error.

Note that while an excess layer of LC is present on the surface of the sample, it does not contribute to the discussed effects, because the electric field exists only within the PBG structure.

Both the polarized light microscopy and PBG reflection tuning experiments demonstrate that the structures fabricated according to the design rules set out in Sections II-A and II-B allow for active material tuning inside high refractive index, conductive PBG structures.

Fig. 5. Intensity of transmitted polarized light versus applied electrical voltage for a 15-µm-thick PBG membrane. The schematics of the polarized light microscopy measurement is shown to the right of the graph. Schematic orientation of LC molecules inside the pores before and after the switching is also shown inside the graph.

Fig. 6. Redshift of the bandgap edge versus applied voltage for 60-µm-thick PBG structure. The bandgap edge is centered around 1300 cm\(^{-1}\). The solid line is the guide for an eye. The schematics of the measurement is shown to the right of the graph.
The two types of structures that were tested varied in thickness and aspect ratio. However, the electric fields required to initiate switching were very similar (around 0.7–0.8 V/μm) which demonstrates that there is no field attenuation in the middle of the PBG layer. This value is only slightly higher than that required for bulk reorientation of E7 LC in the conventional sandwich-cell geometry [14]. The increase can be attributed to greater confinement of the LC molecules within the pores. Because the required operating voltage can be reduced linearly by downsampling the thickness of the device, a typical integrated PBG device with a thickness of 1 μm could have a threshold voltage as low as 0.5–1 V.

V. Conclusion

Tunability in high refractive index-contrast PBG structures is a highly desirable feature for future integrated photonics applications. However, the free carrier electric field screening effect can significantly hamper its utility. In this paper, the equivalent circuit method was used to analyze the electric field distribution inside a 2-D PBG structure. Appropriate design parameters have been suggested that will essentially eliminate the electric field screening effect and maximize the device tunability. First, to provide a uniform field distribution, it is necessary to place the electrodes in direct contact with the semiconductor host. Second, to avoid excessive power consumption, it is necessary to maximize the resistivity of the semiconductor host by decreasing the carrier concentration and mobility. To experimentally confirm the proposed concepts, LC-filled macroporous silicon 2-D PBG structures were designed and fabricated. Finally, electrical tuning of LCs inside the PBG structures was demonstrated using polarized light microscopy and PBG reflection analysis. Experimental results indicate that the free-carrier electric field screening effect has indeed been eliminated in the fabricated devices. The electric field required to initiate switching in the fabricated structures is only 0.7–0.8 V/μm, which is promising for the CMOS applications.

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References

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